Ordering number:EN3665

NPN Triple Diffused Planar Silicon Transistor

2SC4769

Ultrahigh-Definition Color Display Horizontal Deflection Output Applications

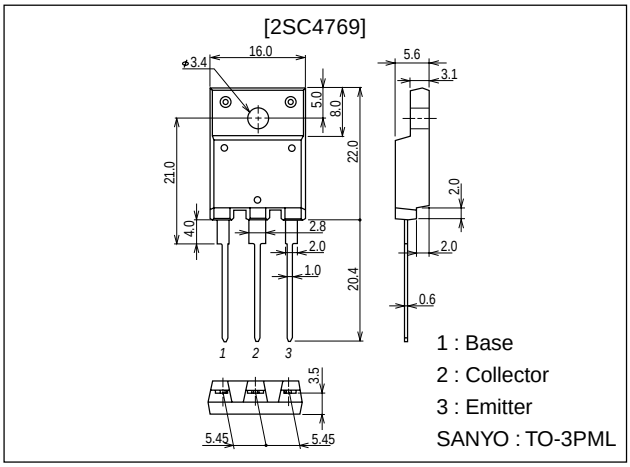
Features

- High speed (t_f=100ns typ).
- High breakdown voltage (V_{CBO}=1500V).
- High reliability (Adoption of HVP process).
- Adoption of MBIT process.
- On-chip damper diode.

Package Dimensions

unit:mm

2039D



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		1500	V
Collector-to-Emitter Voltage	V_{CEO}		800	V
Emitter-to-Base Voltage	V_{EBO}		6	V
Collector Current	I_C		7	A
Collector Current (Pulse)	I_{CP}		16	A
Collector Dissipation	P_C		3	W
		Tc=25˚C	60	W
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=800V, I_E=0			10	μA
	I_{CES}	V_{CE}=1500V, R_{BE}=0			1.0	mA
Collector-to-Emitter Sastain Voltage	$V_{CEO(sus)}$	I_C=100mA, I_B=0	800			V
Emitter Cutoff Current	I_{EBO}	V_{EB}=4V, I_C=0	40		130	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=5A, I_B=1.7A			5	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=5A, I_B=1.7A			1.5	V

* : The 2SC4769 is classified by 5A h_{FE} as follows :

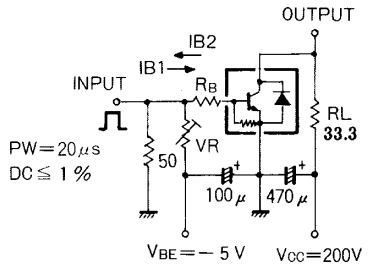
h_{FE}	3 to 5	4 to 6	5 to 8
Rank	1	2	3

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquaters

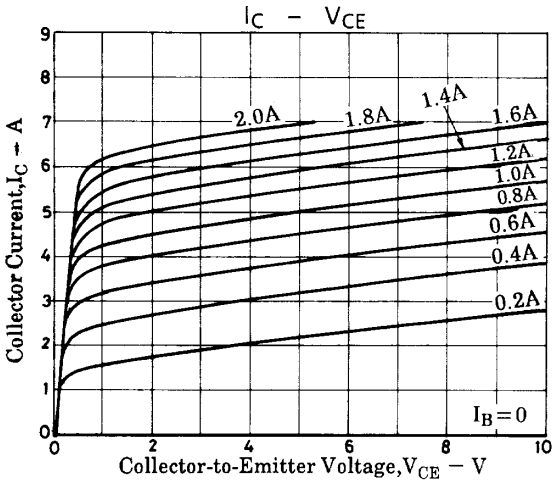
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

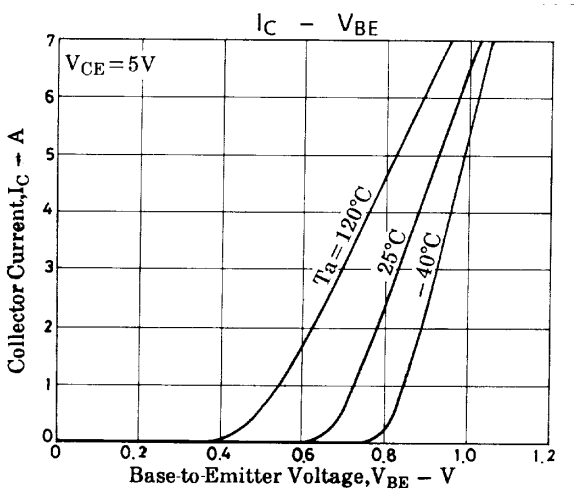
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DC Current Gain	$h_{FE}1$	V_{CE}=5V, I_C=1A	8			
	$h_{FE}2$	V_{CE}=5V, I_C=5A	3.0*		8.0*	
Diode Forward Voltage	V_F	I_{EC}=7A			2.0	V
Storage Time	t_{stg}	I_C=4A, I_{B1}=0.8A, I_{B2}=–1.6A			3.0	μs
Fall Time	t_f	I_C=4A, I_{B1}=0.8A, I_{B2}=–1.6A		0.1	0.2	μs

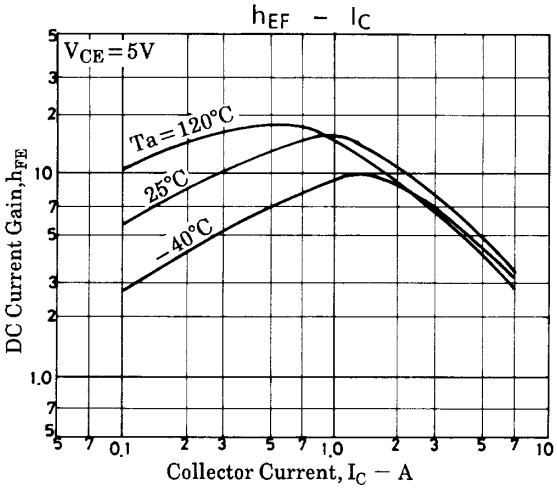
Switching Time Test Circuit

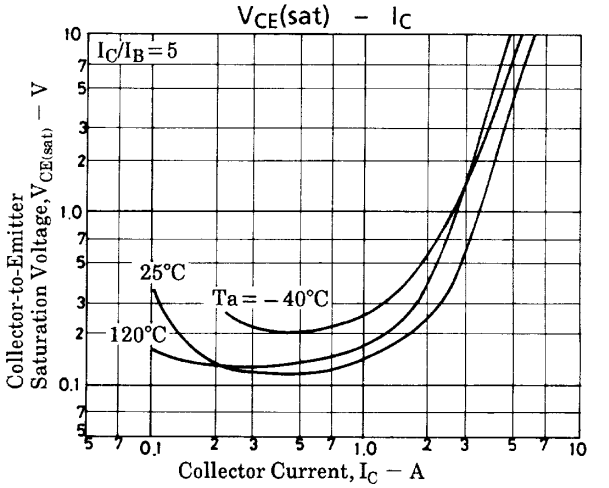


Unit (resistance: Ω, capacitance: F)

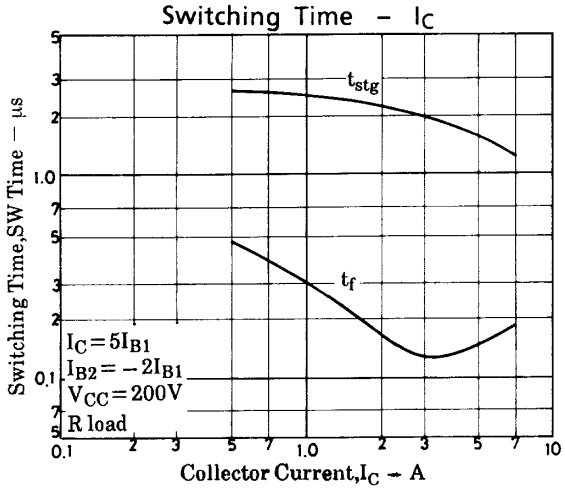




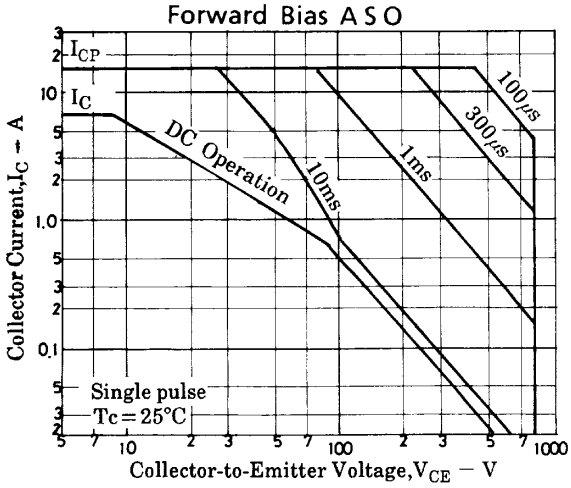




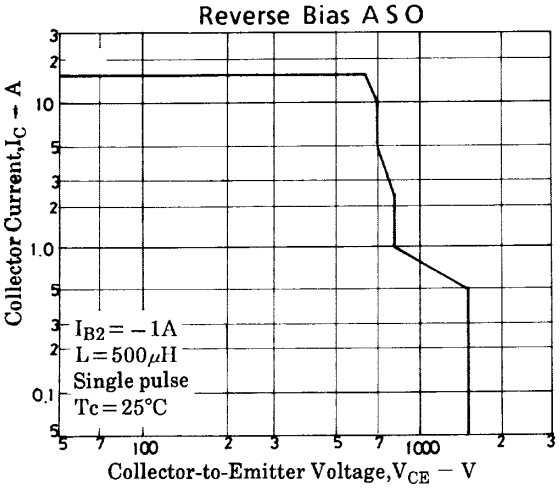
Switching Time – I_C



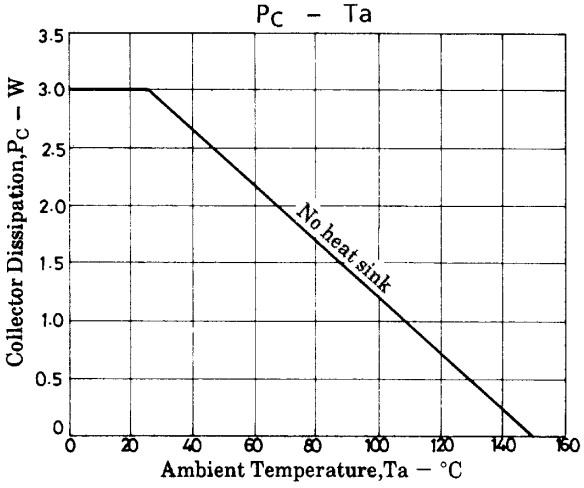
Forward Bias A S O



Reverse Bias A S O



P_C – Ta



P_C – Ta