

(6N138)

MAXIMUM RATINGS* (Ta = 0°C to +70°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Note 1)	I _F	20	mA
	Pulse Forward Current	I _{FP} ^{*1}	40	mA
	Total Pulse Forward Current	I _{FP} ^{*2}	1	A
	Reverse Voltage	V _R	5	V
	Diode Power Dissipation (Note 2)	P _D	35	mW
DETECTOR	Output Current (Note 3)	I _O	60	mA
	Emitter-Base Reverse Voltage	V _{EB}	0.5	V
	Supply Voltage	V _{CC} ^{*3}	-0.5 to 18	V
	Output Voltage	V _O ^{*3}	-0.5 to 18	V
	Output Power Dissipation (Note 4)	P _O	100	mW
Operating Temperature Range		T _{opr}	0 to 70	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Solder Temperature (10s) ^{*4}		T _{sol}	260	°C
Isolation Voltage (1min., R.H. ≤ 60%)		BV _S ^{**}	2500	V _{rms}
			3540	V _{dc}

- * JEDEC Registered Data
- ** Not Registered JEDEC
- *1 50% duty cycle, 1ms pulse width
- *2 Pulse width 1μs, 300pps
- *3 6N138... -0.5 to 7V
- *4 1.6mm below seating plane

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ELECTRICAL CHARACTERISTICS

OVER RECOMMENDED TEMPERATURE ($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	*5TYP.	MAX.	UNIT
Current Transfer Ratio (Note 5, 6)	6N139	CTR*	$I_F = 0.5\text{mA}$, $V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$	400	800	—	%
	6N138		$I_F = 1.6\text{mA}$, $V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$	500	900	—	
Logic Low Output Voltage (Note 6)	6N139	V_{OL}	$I_F = 1.6\text{mA}$, $I_O = 6.4\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
			$I_F = 5\text{mA}$, $I_O = 15\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	
			$I_F = 12\text{mA}$, $I_O = 24\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.2	0.4	
	6N138		$I_F = 1.6\text{mA}$, $I_O = 4.8\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	
Logic High Output Current (Note 6)	6N139	I_{OH}^*	$I_F = 0\text{mA}$, $V_O = V_{CC} = 18\text{V}$	—	0.05	100	μA
	6N138		$I_F = 0\text{mA}$, $V_O = V_{CC} = 7\text{V}$	—	0.05	250	
Logic Low Supply Current (Note 6)		I_{CCL}	$I_F = 1.6\text{mA}$, $V_O = \text{Open}$ $V_{CC} = 5\text{V}$	—	0.2	—	mA
Logic High Supply Current (Note 6)		I_{CCH}	$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 5\text{V}$	—	10	—	nA
Input Forward Voltage		V_F^*	$I_F = 1.6\text{mA}$, $T_a = 25^\circ\text{C}$	—	1.65	1.7	V
Input Reverse Breakdown Voltage		BV_R^*	$I_R = 10\mu\text{A}$, $T_a = 25^\circ\text{C}$	5	—	—	V
Temperature Coefficient of Forward Voltage		$\Delta V_F / \Delta T_a$	$I_F = 1.6\text{mA}$	—	-1.9	—	mV/ $^\circ\text{C}$
Input Capacitance		C_{IN}	$f = 1\text{MHz}$, $V_F = 0$	—	60	—	pF
Resistance (Input-Output)		R_{I-O}	$V_{I-O} = 500\text{V}$ (Note 7) R.H. $\leq 60\%$	—	10^{12}	—	Ω
Capacitance (Input-Output)		C_{I-O}	$f = 1\text{MHz}$ (Note 7)	—	0.6	—	pF

** JEDEC Registered Data.

*5 All typicals at $T_a = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$, Unless otherwise noted.

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SWITCHING SPECIFICATIONS (Ta = 25°C, V_{CC} = 5V, Unless otherwise specified)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to Logic Low at Output (Note 6, 8)	6N139	t _{pHL} *	1	I _F = 0.5mA, R _L = 4.7kΩ	—	5	25	μs
	6N138			I _F = 12mA, R _L = 270Ω	—	0.2	1	
				I _F = 1.6mA, R _L = 2.2kΩ	—	1	10	
Propagation Delay Time to Logic High at Output (Note 6, 8)	6N138	t _{pLH} *	1	I _F = 0.5mA, R _L = 4.7kΩ	—	5	60	μs
	6N139			I _F = 12mA, R _L = 270Ω	—	1	7	
				I _F = 1.6mA, R _L = 2.2kΩ	—	4	35	
Common Mode Transient Immunity at Logic High Level Output (Note 9)		CM _H	2	I _F = 0mA, R _L = 2.2kΩ V _{CM} = 400V _{p-p}	—	500	—	V / μs
Common Mode Transient Immunity at Logic Low Level Output (Note 9)		CM _L	2	I _F = 1.6mA, R _L = 2.2kΩ V _{CM} = 400V _{p-p}	—	-500	—	V / μs

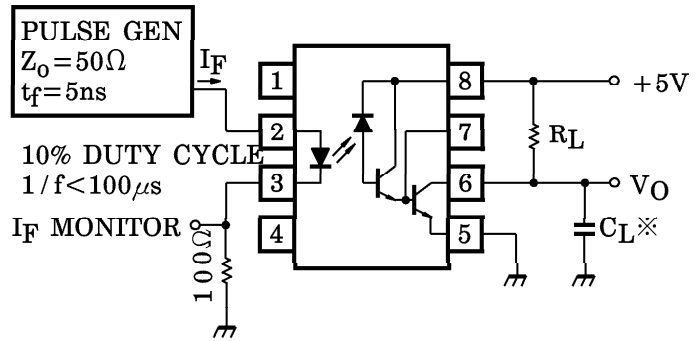
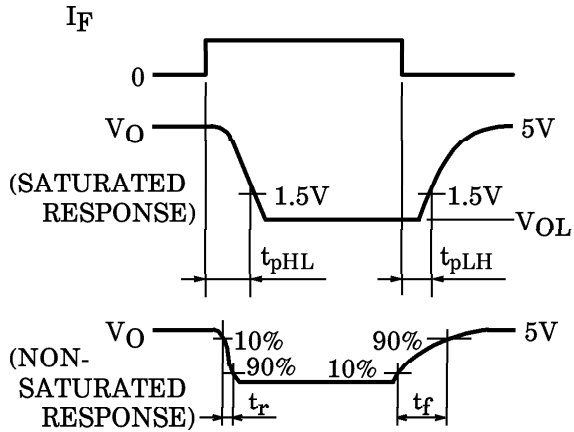
* JEDEC Registered Data.

NOTES :

- Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
- Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
- Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
- Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
- DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
- Pin 7 Open.
- Device considered a two-terminal device : Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
- Use of a resistor between pin 5 and 7 will decrease gain and delay time.
- Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V).
Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).

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TEST CIRCUIT 1.



* C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2.

